in each of said memory regions, said memory transistors are arranged in said one direction;

in each of said element separating regions, an element separating insulating film is formed on said substrate, and extends in said one direction;

each of said floating gates is not formed on said element separating regions, but formed only on each of said memory transistors in said memory regions;

said control gates extending in a direction perpendicular to said one direction and intersecting said memory regions and said element separating regions, each said control gate being arranged on said element-separating insulating films in said element separate regions;

in each said memory region, both said oxide film and another oxide film are formed between each said side wall and each said floating and control gates, and are formed between each said side wall and said substrate; and

in each said element separating region, both said oxide film and said another oxide film are formed between each said side wall and each said floating and control gates, and only said another oxide film is formed between each said side wall and each element separating insulating film.--

REMARKS:

This is in response to the Office Action dated December 28, 1999 (paper #7). Pursuant to this amendment, claims 5-7 and 16-17 are pending in the present application. Reexamination and reconsideration are respectfully requested.

Applicant replaces original claims 1 and 2 with new independent claim 16, which generally includes the same limitations as prior claim 2, rewritten in part for additional clarity.

The outstanding Office Action rejects prior claims 1-7 as obvious over U.S. Patent No. 5,834,807 to Kim taken in view of U.S. Patent No. 5,068,697 to Noda, et al., and further taken in view of U.S. Patent No. 5,907,171 to Santin, et al. Applicant submits that claim 16 and its dependent claims distinguish over these references and are in condition for allowance.

The present application describes a structure for the memory transistors of a nonvolatile memory device well illustrated in FIG. 11(a) of the application. One memory transistor includes a source 7a, a drain 7b and a gate structure including a gate oxide 3, a floating gate 4, an interlayer dielectric 5 and a control gate 6. In this figure, the control gate is formed of doped

polysilicon and a conductivity enhancing silicide layer 9. Along the sides of the gate structure are a multilayer insulating structure including an oxide layer (31, 32, FIG. 7(a)) on the walls of the gate structure, silicon nitride side walls or spacers 10 and an overlying silicon nitride layer 11. The second silicon nitride film 11 covers the upper part of the control gate 6 including the silicide layer 9 and the outer surfaces of the silicon nitride spacers 10.

The structure shown in FIG. 11(a) provides a number of advantages to the overall memory device. Because two layers of silicon nitride are used to cover the walls of the gate structure, the diffusion of performance degrading impurities into gate electrodes 4 and 6 can be reduced. This two silicon nitride film structure also facilitates the use of plasma CVD to deposit the upper silicon nitride film 11, which provides a denser a higher quality film at a low temperature. Were the side walls 10 not made of silicon nitride, the use of plasma CVD to deposit a high quality upper silicon nitride film 11 would not be desirable, as the plasma deposition process would introduce impurities into the gates 4 and 6. Finally, the inner protective oxide film (31, 32, FIG. 7(a)) on the walls of the gate structure is useful in limiting the diffusion of impurities such as hydrogen into the gates and channel region.

These advantageous aspects of the application's device are reflected in new independent claim 16, which recites:

> "an oxide film formed on said substrate and at least on both sides of each said floating gate and both sides of each said control gate;
>
> side walls each for protecting sides of said floating gate and said control gate of each said transistor, each said side wall formed from a first silicon nitride film formed by low-pressure CVD over said oxide film;
>
> a second silicon nitride film covering surfaces of said control gate and each of said side walls of each of said memory transistors and on surfaces."

None of the references of record describe or suggest such a three-layer structure along the sides of floating gate and control gate structures of nonvolatile memory transistors.

The primary reference cited against the present application is Kim patent. FIG. 6 of the Kim patent shows the transistor structure of that patent. Each of the gate stacks (44, 46, 48, 50, 52) has a layer 62 on each of its side surface. A conductor 66 is provided between adjacent layers 62. The Kim patent does not disclose what material is used for the layer 62 and does not

teach a multiple layer structure. Consequently, the Kim patent does not describe the three layer (oxide, nitride and nitride) structure defined by the quoted claim language above.

The Office Action states that it would have been obvious to replace the layer 62 with silicon nitride. Applicant respectfully disagrees. As discussed in the present application at page 2 of the application, the deposition of silicon nitride yields hydrogen that diffuses into polysilicon gate electrodes and these impurities make device performance unpredictable and poorly controlled. Those of ordinary skill in this art would appreciate that fact and would consequently avoid using silicon nitride for the layer 62.

The Office Action relies on the Noda patent as a secondary reference. The Noda patent does not suggest modifying the Kim patent so as to yield the claimed structure. As illustrated in, for example FIG. 4, the Noda patent teaches the use of a three-layer structure, generally analogous to the layer structure defined in claim 16 of the present application. The Noda patent's structure includes an oxide layer 25, an oxide side wall 26 and a nitride layer 29. To the extent that the Noda patent suggests modifying the structure of the Kim patent, it would be to replace the one layer 62 with the three layers of the Noda patent. That structure would not, however, meet the limitations of claim 16. Rather, the result of combining the Kim patent with the Noda patent would be the structure including an oxide side wall described as disadvantageous in the background of the present application. As such, the combination of the Kim patent and the Noda patent does not yield the invention of claim 16. Claim 16 distinguishes over the proposed combination by reciting the three layer (oxide, nitride, nitride) structure set forth in the quoted language of claim 16.

The other cited references do not address the deficiencies of the proposed combination of the Kim patent taken in view of the Noda patent. Applicant consequently submits that claim 16 and its dependent claims 5-7 and 17 distinguish over the art of record and are in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number 310-282-2000 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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